CCB Systems Tests

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I. Introduction & Detector Signal Characteristics

This document presents a range of tests for the CCB. Probably not all of these tests will be needed, and we may find we need to do some that haven't been thought of. Our present purpose is to provide a framework.

The acquisition of data will be commanded via the YGOR manager using the CLEO interface. There are two modes in which data can be acquired:

- Normal integration or scan mode: each integration returns *n* x *m* 32-bit words where *n* is the number of CCB input ports (16) and *m* is the number of phase switch states (1-4). Note that the YGOR manager permits the selective enablement & disablement of individual ports, which determines whether that port's data are recorded to the FITS file. When dealing with "normal" data, we define the quantity $\Delta = \frac{1}{2} (d^{00} + d^{11} - d^{01} - d^{10})$ for two active switches, or $\Delta = d^0 - d^1$ for one active switch, to denote the measured power difference for the given integration. The superscripts here denote phase switch control line state.
- Raw data (dump mode): A stream of raw ADC samples. You must specify a single daughter card and a single ADC on the daughter card to look at. A fixed number of sequential samples are returned from the beginning of an integration; this can be repeated indefinitely over integrations, or for a fixed number of integrations. Each datum is a 16 bit word. The dump data will be accessible using a TCP/IP service in the CCB server. Using this from a C program we could either analyze dump-mode data on the fly, or write out files in whatever format you like, to analyze them later with IDL, gnuplot, etc. (ending up in a file somewhere in some convenient, to be specified binary format).

Data will be examined with custom utilities (probably written in IDL) developed by Brian & others.

For reference, some characteristics of the detector circuit and the signal received by the CCB are:

- Input signal: balanced differential signals swinging over 5V range, between –2.5V and +2.5V, with common-mode voltage in the range 1.0V to 3.2V.
- Tsys (min): 35-40 K (RMS noise across a 3.5 GHz detected RF band of 0.8m K, in one second integration).
- Tsys (max): 433 K (3.5GHz bandwidth, 11 bits ADC dynamic range, 3 bits to allocate noise, 50 K Tsys, low-pass filter time constant of 0.25 u sec).
- ADCs: 11 bits dynamic range; it includes 3 bits to allocated RMS noise.
- Counts/Volts gain: 410 (2^{11} / 5) (although we keep all the 14 bits).
- Counts/Kelvin gain: 4.7 (2^{11}/ 433).
- Noise RMS: 3 bits, 8 counts, 19.5m V, 6.3u V/√(Hz) averaged over a 10 MHz bandwidth (0.1u Sec samples).

- Differential Driver Gain (AD8138) due to impedance matching: 2.
- Minimum supported integration time: 1m sec.

Generally the unique new functionality of the CCB + Ka band is **excellent noise performance** (for measuring bright sources you can already use the DCR) so when in doubt, testing should focus more on this rather than things like dynamic range; and the most relevant operating range is Tsys(min) as opposed to Tsys(max) or something in between. Also we only expect this excellent performance from the **differenced** data, so here also, basic health checks for total power are in order but performance metrics should focus on the differenced data.

We define a nominal test mode for acquiring normal integration data as per the following table. This can be set up in CLEO's CCB screen (Advanced tab), and we refer to it at the "nominal integration configuration". It corresponds to full 2 phase-switch switching at 20 kHz with an integration time of 0.1 sec.

A nominal integration configuration is:

ADC Samples per phase switch state	250
Phase switch states per phase cycle	4
Phase switch cycles per integration	1000
Active Switches {none, A, B, both}	Both
Closed (phase) switches (at scan start)	Both
Cal {Off, Left, Both, Right} integrations	{10,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	Best value
Holdoff	7 (7+1=8x256 clock cycles= 0.2ms)
Phase switch delay	Best value
ADC Delay	Best value
Active ports	All
Sample type {ADC, FAKE}	ADC

A nominal configuration for a dump mode scan is:

Samp per state	16383
Phase switch states per phase cycle	1
Phase switch cycles per integration	1
Active Switches {none, A, B, both}	None
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{0,0,0,0}
Cal {rise, fall} flagging	{0,0}
Dump Port	As desired
Dump Max samples	16383
Dump Max integs	1

Round trip delay	Best value
holdoff	7 (or 0.2m sec)
Phase switch delay	Best value
ADC delay	Best value
Sample type {ADC, FAKE}	FAKE

General comments:

- In any of the tests where noise performance is an issue, it would be sensible to seal up the CCB and use cables as similar to the final configuration as feasible.
- It is worth bearing in mind that tests in dump mode must be done port-by-port. Tests in regular integration mode can be done for the whole CCB at once. Probably we want to focus on a few ports for dump mode tests when we can—and spot check other ports—while doing as much of the actual performance testing in regular mode as feasible. For CCB-only tests (no receiver), though, we may be limited by the number of input test signals to the backend.
- When acquiring dump-mode data, you'll have to be organized & keep track of the data files in synch with your own notes.
- When acquiring regular scan-mode data, CLEO allows you to set things like the source name which will appear in the FITS file, and can be used to help keep the data organized. (It will be confirmed where the real data go: /home/simdata/JUNK/CCB/ ?)

II. Test 1: Pseudo-random Samples

The purpose of this test is to verify that the master & slave FPGAs process digital data as expected (no receiver connected). It will also check that the pseudo-random sample generators work properly. Note that the pseudo-random sample generator is of capable presenting $2^{14} - 1$ **different** samples, or 16383 samples. The sequence of pseudo-random samples is fixed (with a known start count) and it's repeated for each integration. There will be two components to this test:

- A dump test—which verifies that the pseudo-random sequence is as expected.
- Regular integration tests—which allows us to check the full system in normal operating mode against a known answer.

For the dump test configure the system per the test configuration of Section I. Set dump_lim_reg to 16383 samples. Set none of the phase-switches as active (2^0=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 16383 (~1.64m sec). Set the integration time ~ 1.64m sec, that is 1 cycle per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to zero (no A/D conversion is made in this test). No cal-diode set. Collect 16383 dump samples (~1.64m sec). Write the streamed dump data to a file. Compare the result to what Martin's sequence generator program predicts (the fake pseudo-random sequence: ~mshepher/bin/ccb_fake_samples).

For the next test in normal scan mode, we would like to check if the accumulators in the bins are working properly (without phase-switching). Set none of the phase-switches as active (2^0=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 16383 (~1.64m sec). Set the integration time ~ 16.4m sec, that is 10 cycle per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to zero (no A/D conversion is made in this test). No cal-diode set. Collect 100 integrations (1.64 sec). Since the pseudo-random sequence repeats for every integration, every integration should have the same value, and we can predict this value exactly (1,342,095,360 counts, using Martin's integration generator program: ~mshepher/bin/ccb_fake_integ). This will also check the data representation in the FITS file.

Normal scan mode:

ADC Samples per phase switch state	16383
Phase switch states per phase cycle	1
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	None
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{100,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC Delay	0 (no AD conversion)
Active ports	As desired
Sample type {ADC, FAKE}	FAKE

In order to test the phase-switch bins during normal scan mode, for the next test set one of the phase-switches as active (2^1=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 16383 (~1.64m sec). Set the integration time ~ 16.4m sec, that is 5 cycle per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to zero (no A/D conversion is made in this test). No cal-diode set. Collect 100 integrations (1.64 sec). As we said before, since the pseudo-random sequence repeats for every integration, starting always at the same value, therefore each integration should have the same value (671,047,680 counts for each bin). This means that the differenced data for a given integration ($\Delta = d^0 - d^1$) should be zero (check using Martin's integration generator program: ~mshepher/bin/ccb_fake_integ). The superscripts here denote phase switch control line state. This will also check the data representation in the FITS file.

Normal scan mode:

ADC Samples per phase switch state	16383

Phase switch states per phase cycle	2
Phase switch cycles per integration	5
Active Switches {none, A, B, both}	A (or B, as desired)
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{100,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	~0 (no receiver connected)
ADC Delay	0 (no AD conversion)
Active ports	As desired
Sample type {ADC, FAKE}	FAKE

Furthermore we could check that the integration registers overflow when we expect them to. Again, this can be predicted, based on the pseudo-random sequence generator program (using Martin's integration generator program: ~mshepher/bin/ccb_fake_integ). For one signal injector sequence, if you add 16383 samples, the resulting integration value (with no phase-switches active) should be 134,209,536 counts. Because within the integrators, each accumulator has an adder with 32 output bits, and the input samples are 14 bits length, we would be capable to add around 32 (a total of 4,294,705,152 counts) consecutive pseudo-random sequences before saturating the integrator. Therefore, for the next test, set one of the phase-switches as active (2^1=2 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 16383 (~1.64m sec). Set the integration time ~ 104.85m sec, that is 32 cycle per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to zero. No cal-diode set. This should be the maximum integration time before saturating the integrators.

Normal scan mode:

ADC Samples per phase switch state	16383
Phase switch states per phase cycle	2
Phase switch cycles per integration	32
Active Switches {none, A, B, both}	A
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{32,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC Delay	0 (no AD conversion)
Active ports	As desired
Sample type {ADC, FAKE}	FAKE

Note 1: Order of the Dump samples

About the order of the Dump samples being streamed to the cpu. According to Martin's design, the sequence of the phase-switches (according to what you set in the corresponding parameters) is selected trough the MUX1 (diagram 3.36, "ccb_fpga_design" document). For example:

active_b=0, active_a=1, closed_b=1, closed_a=0 (start_scan_reg register)

Then, this setup selects sequence d6:

Phase-switch A: 1010
Phase-switch B: 1111

In order to know the temporal sequence these patterns must be readed from right to left. Then, the first state_len samples would correspond to:
Phase-switch A = 0 (off)
Phase-switch B = 1 (on)

Then, the following state_len samples would correspond to:
Phase-switch A = 1 (on)
Phase-switch B = 1 (on)

Then, the following state_len samples would correspond to:
Phase-switch A = 0 (off)
Phase-switch B = 1 (on)

Then, the following state_len samples would correspond to:
Phase-switch A = 1 (on)
Phase-switch B = 1 (on)

Note 2: Martin's generator programs

Martin's sequence generator program: ~mshepher/bin/ccb_fake_samples

If no arguments are specified, then this displays the samples of one full sequence of 16383 fake values. Alternatively, if an integer command-line argument is specified, then this is interpreted as the number of samples to display. Note that the displayed sequence starts from the sample that the CCB fake-sample generator outputs at the start of each integration period.

Martin's integration generator program: ~mshepher/bin/ccb_fake_integ

The following is an example of how to use this:

~mshepher/bin/ccb_fake_integ -state_len 16383 -active_switches a -closed_switches none -blank_dt 0 -integ_len 32

When invoked as above, the program prints the following:

The selected scan configuration parameters are:
active_switches=a
closed_switches=none
state_len = 16383 x 100ns
integ_len = 32 (phase-switch cycles)
blank_dt = 0 x 100ns

The phase-switch integration totals should be
4294705152 4294705152 0 0

The integration totals scaled to ADC units should be
08192.00000 08192.00000 00000.00000 00000.00000

Note that in the above case the values in the two active phase-switch bins, are identical. This is because the length of each phase-switch state has been specified as equaling the length of the fake sample sequence, such that the samples repeat from one state to the next. In general, with different values for the state_len argument, this won't be the case.

III. Test 2: DC Inputs

The purpose of this test is to establish the ADC calibration (without the receiver), set detector circuit levels, and verify that the CCB itself is contributing an acceptable amount of noise to the signal (no phase-switching & no receiver connected).

For this test put a range of DC levels into a CCB input port:
433 K (Hint: saturation, be sure that no damage will be produced!) 2.5 Vd /2
400 K (near saturation) 2.12 Vd /2
112K (~ LN2 + Tsys min) -1.21 Vd /2
100 K (~cold load) -1.35 Vd /2
35 K (~Tsys min) -2.10 Vd /2

The input DC noise must be << 0.4% Vfs (-47db). Due to impedance matching, we should have less than 19.5mV / 2 = 9.75m V (0.2% Vfs) or -54.2db at the CCB input port (HINT: differential driver has a gain = 2, with 78Ω impedance, to match cable impedance). DC input signal should be stable for more than 1 sec. To transform both AC and DC signals into the correct format for the analog inputs we should use the specially modified detector module of the lab.

In dump mode (selecting always the same sampler of the same daughter card) set dump_lim_reg to 2000. Set none of the phase-switches as active (2^0=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 1000 (0.1m sec). Set the integration time ~1m sec, that is 10 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to 20n sec (recommended). No cal-diode set. Collect at least 10000 dump samples (5 x 1m sec integrations) for each input voltage value.

Dump mode:

Samp per state	1000
Phase switch states per phase cycle	1
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	none
Closed (phase) switches (at scan start)	none
Cal {Off, Left, Both, Right} integrations	{5,0,0,0}
Cal {rise, fall} flagging	{0,0}
Dump Port	As desired
Dump Max samples	2000
Dump Max integs	5
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC delay	20ns
Sample type {ADC, FAKE}	ADC

With that data plot the mean ADC level at each input voltage, versus input voltage. This should be a straight line up to near saturation. One should also check the RMS of the ADC samples; we would like this to be much less than 8 counts but it's not formally specified (it's a total power, not a switched power). The power spectrum of the ADC samples should also be examined; but here too there could easily be harmonics of 60 Hz quite prominent in the total power data that don't affect the CCB switched performance at all.

We may also want to acquire data in the regular scan mode (which has the advantage of returning all 16 ports at once instead of one at a time). In normal scan mode set none of the phase-switch as active (2^0=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 1000 (0.1m sec). Set the integration time ~1m sec, that is 10 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to 20n sec (recommended). No cal-diode set. Collect 100 integrations (100m sec). Because the integration data (with not phase-switching) will be the accumulation of 10 x 1000 ADC samples, we can scale the integrations to the nominal input voltage value dividing each integration value for 10 x 1000. From the data of the FITS files, plot the averaged of the scaled integrations for each input DC level v/s the input DC level (this also should be a straight line up to near

saturation). Plot the mean of the scaled integrations for each input voltage (100 integration per input DC level), to estimate the RMS value of noise for each input DC level.

Normal scan mode:

ADC Samples per phase switch state	1000
Phase switch states per phase cycle	1
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	none
Closed (phase) switches (at scan start)	none
Cal {Off, Left, Both, Right} integrations	{100,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC Delay	20ns
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

Do the above described analysis with all of the 16 active ports.

IV. Test 3: Determine the ADC Delay

The purpose of this test is to determine an appropriate value for the ADC delay (no receiver connected). The ADC delay is the phase shift of the ADC clock relative to the FPGA master clock; it is settable in increments of 10 ns.

Configure the system as for the DC level tests (set to midlevel). For a single ADC on a single daughter card, acquire dump data with a range of ADC delays (from 0 ns to 50 ns say).

In dump mode set dump_lim_reg to 2000 ADC samples. Always select the same sampler of the same daughter card. No cal-diode set. Also set none of the phase-switch as active (2^0=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 2000 (0.2m sec). Set the integration time ~2m sec, that is 10 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Collect at least 6000 dump samples for each test (3 x 2m sec integrations). Write the streamed dump data to files.

Dump mode:

Samp per state	2000

Phase switch states per phase cycle	1
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	None
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{3,0,0,0}
Cal {rise, fall} flagging	{0,0}
Dump Port	As desired
Dump Max samples	2000
Dump Max integs	3
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC delay	0, 10ns, 20ns, 30ns, 40ns, 50ns
Sample type {ADC, FAKE}	ADC

We must read out the ADCs within the time window that is specified in the AD9240 data-sheet (8n s < ADC delay < 19n s). If not, then the ADC output could do anything, and the resulting values would probably be uncorrelated with the ADC input signal.

We should use an oscilloscope to find out what the actual delay between the phase-shifted and un-phase-shifted clocks is, and from this figure out the range of the ADC-delay configuration parameter that meets the requirements in the AD9240 data sheet. It's not necessary to experiment with taking data for values outside of this range, since even if for one ADC, we managed to get a good noise level from a delay that was out of spec, we might get nothing at all out of a different ADC of the same type.

Examine the dump data (crosscheck); when the ADC delay is too long or too short, the ADC will not have enough time to properly acquire data before the slaves FPGAs start to read the ADC output. Therefore, we expect the data will not be as good (we may just need to experiment). With that data calculate the mean and RMS of the ADC level for the input voltage, for each ADC delay value. We would prefer the ADC delay that fulfill the AD9240 requirements and that produce a lower RMS (also it should be less than 8 counts but it's not formally specified). Repeat this procedure with all the input ports, and select the largest delay from all of the ADC delays.

For all subsequent tests use the best determined value of the ADC delay.

V. Test 4: Round trip delay w/o receiver (optional)

The purpose of this test is to determine the roundtrip delay of the phase-switch control signal but without the receiver connected. It means that we will only be able to determine a lower limit of the roundtrip delay, but it will be done very precisely.

The strategy is to feed one of the phase-switch control signals back into an input port, and then fiddle with the roundtrip time parameter, while looking at the dump-mode outputs, to make sure that it can be used to reliably direct the high state of the control output into a particular bin.

The timing ticks that govern data-acquisition are correctly delayed with respect to those that generate the receiver control signals, by the amount of time that it takes for the effects of toggling phase-switches and cal-diode states to propagate to the slave FPGAs. i.e. the roundtrip. Therefore, with the proper roundtrip delay, and having at least one of the phase-switch active, and feeding it back to one input port, we should see a High level signal in only one bin, while the other bin should be at Low level.

In dump mode set dump_lim_reg to 2000 ADC samples. Always select the same sampler of the same daughter card. No cal-diode set. Also set one of the phase-switch as active (2^1=2 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 1000 (0.1m sec). Set the integration time ~2m sec, that is 10 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to the best one. Collect at least 6000 dump samples for each test (3 x 2m sec integrations). Write the streamed dump data to files. Repeat this test for different values of the roundtrip parameter. The main goal is to get a High level signal (counts) in one bin, that exactly match the duration of the phase-switch state, and a low level signal (counts) in the other bin. For this test we should have an interfacing cable to adapt properly the phase-switch control signal from the DB15 control port into the BNC input port.

Dump mode:

Samp per state	1000
Phase switch states per phase cycle	2
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	A (or B, as desired)
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{3,0,0,0}
Cal {rise, fall} flagging	{0,0}
Dump Port	As desired
Dump Max samples	2000
Dump Max integs	3
Round trip delay	[700n sec – 25u sec]
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC delay	Best value
Sample type {ADC, FAKE}	ADC

VI. Test 5: CCB Noise Level

The purpose of this test is to establish verify that the CCB itself is contributing an acceptable amount of noise to the signal (no receiver connected).

For this test put a range of DC levels into a C CB input port:
112K (~ LN2 + Tsys min) -1.21 Vd /2
100 K (cold load) -1.35 Vd /2
35 K (Tsys min) -2.10 Vd /2

We want to check the noise performance with a DC input level. Because there is no receiver attached the subtracted signal of a single port should be around zero (Example: Δ(1 switch)= 0 + noise). To transform both AC and DC signals into the correct format for the analog inputs we should use the specially modified detector module of the lab.

In normal scan mode, set just 1 phase-switch as active (2^1=2 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 1000 (0.1m sec). Set the integration time ~1m sec, that is 5 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to the best one. No cal-diode set. Collect 100 integrations (100m sec).

Normal scan mode:

ADC Samples per phase switch state	1000
Phase switch states per phase cycle	2
Phase switch cycles per integration	5
Active Switches {none, A, B, both}	A (or B, as desired)
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{100,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	~0 (no receiver connected)
ADC Delay	Best value
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

From the data of the FITS files, check that:

The output level (integration) of the port should agree with the input DC levels (in order to scale the integrations properly, recall that each integration corresponds to 5 x 2 x 1000 "integrated" ADC samples).
Δ(1 switch)= $d^0 - d^1 \sim 0$ (+ noise)
RMS noise level << 8 counts

Repeat this test with both phase switches active, and a range of phase switching frequencies (20 kHz – 250 samples/phase-switch, 10 kHz – 500 samples/phase-switch, 5 kHz – 1000 samples/phase-switch, 1 kHz – 5000 samples/phase-switch). Take care of not saturate the integrators when selecting the integration time.

VII. Test 6: Signal Generator Inputs

The purpose of this test is to verify that the dynamic response of the CCB is acceptable (no receiver connected).

Put a sinusoidal wave signal into the CCB input (input port):

Sinusoidal wave (bipolar differential wave, each output with common mode voltage of 2.5V)
Sinusoid freq. **10K Hz** (first test) and **10 Hz** (second test) (<< 10 MHz)
Sinusoid amplitude 1Vpp
78Ω cable impedance (for matching impedance, differential driver with gain = 2)
We will need the frequencies of both the 10MHz clock and the 10 KHz signals to be set very accurately. Otherwise the differenced values will not come out as zero, even if the CCB is working perfectly. Therefore, a Digital frequency synthesizer would be preferable. To transform both AC and DC signals into the correct format for the analog inputs we should use the specially modified detector module of the lab.

First test: put a sin wave with 10 KHz frequency in one of the input ports.

In dump mode (selecting always the same sampler of the same daughter card), set just one phase-switch as active (2^1=2 phase-switch or measures per cycle). Set dump_lim_reg to 4000 ADC samples. Set the number of samples per phase-switch state to 2000 (0.2m sec). Set the integration time ~10m sec, that is 25 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Set ADC delay to the best one. Collect at least 8000 dump samples (2 x 10m sec integrations). Write the streamed dump data to a file. Plot the raw data and check that we get the appropriate waveform.

Dump mode:

Samp per state	2000
Phase switch states per phase cycle	2
Phase switch cycles per integration	25
Active Switches {none, A, B, both}	A (or B, as desired)
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{2,0,0,0}
Cal {rise, fall} flagging	{0,0}

Dump Port	As desired
Dump Max samples	4000
Dump Max integs	2
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	~0 (no receiver connected)
ADC delay	Best value
Sample type {ADC, FAKE}	ADC

We also want repeat the test in normal scan mode. Set just 1 phase-switch as active (2^1=2 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 2000 (0.2m sec). Set the integration time ~10m sec, that is 25 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Set ADC delay the best one. Collect 100 integrations (1 sec).

Normal scan mode:

ADC Samples per phase switch state	2000
Phase switch states per phase cycle	2
Phase switch cycles per integration	25
Active Switches {none, A, B, both}	A (or B, as desired)
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{100,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	~0 (no receiver connected)
ADC Delay	Best value
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

From the data of the FITS files, check that:
Δ(1 switch)= $d^0 - d^1 \sim 0$ (+ noise)
RMS noise level << 8 counts
Check also that when plotting the integration values, we get the appropriate waveform (zero level, because the bins contain the same integrated data) plus noise (recall that each integration corresponds to 25 x 2 x 2000 "integrated" ADC samples)

Repeat the test in the nominal integration configuration with some number of signal generator inputs. Slow down the input wave so that you get much integration per waveform period. Check that the FITS file shows the appropriate waveform.

Second test: put a sin wave with 10 Hz frequency in one of the input ports.

During this test, in normal scan mode, because the input frequency is much larger than the integration time, we should be capable to follow the input sin wave form. Therefore, set none phase-switch as active (2^0=2 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 2000 (0.2m sec). Set the integration time ~1m sec, that is 5 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Set ADC delay the best one. Collect 200 integrations (1 sec).

Normal scan mode:

ADC Samples per phase switch state	2000
Phase switch states per phase cycle	1
Phase switch cycles per integration	5
Active Switches {none, A, B, both}	None
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{200,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	~0 (no receiver connected)
ADC Delay	Best value
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

From the data of the FITS files, check that when plotting the integration values, we get the appropriate waveform (sin wave form of 10 Hz frequency) plus noise (recall that each integration corresponds to 5 x 1 x 2000 "integrated" ADC samples). Check also that the RMS noise level << 8 counts

In addition to theses tests, you might also put two distinct waveforms (different shapes, non-commensurate frequencies) into adjacent ports and look at the outputs to measure the amount of crosstalk, if any (see also next test).

VIII. Test 7: Crosstalk test

The purpose of this test is to check the crosstalk profile of adjacent input ports. Send a strong signal (above saturation level, if this won't harm anything), into one input port, via the external twin-ax cable that we intend to use, and a DC mid level into all the other ports, again via the external twin-ax cables.

FIRST TEST:

For this test put a HIGH DC level into a SINGLE CCB input port:
433 K (Hint: saturation, be sure that no damage will be produced!) 2.5 Vd /2

For all other CCB input ports, put the following DC level (use the same DC source for all of input ports): 217K (~ mid level) 0 Vd

The input DC noise must be << 0.4% Vfs (-47db). Due to impedance matching, we should have less than 19.5mV / 2 = 9.75m V (0.2% Vfs) or -54.2db at the CCB input port (HINT: differential driver has a gain = 2, with 78Ω impedance, to match cable impedance). DC input signal should be stable for more than 1 sec.

Then simply integrate data from all of the other ports, to see if they deviate from zero when the high DC level signal is turned on. We should also do it with a noise generator. It would make most sense to analyze the data on the fly, rather than create large files for later analysis. This would allow us to perform long scans.

For this test, set the next normal scan configuration: set the two phase-switches as active (2^2=4 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 2000(0.2m sec). Set the integration time ~200m sec, that is 250 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Set ADC delay to the best one. Collect at least 500 integrations (100 sec). Start the integrations with the High DC Input generator turned off, and the rest of the input port set to mid level. After the first 5 seconds from starting the integrations, turn on the High DC input, while keep integrating samples.

Normal scan mode:

ADC Samples per phase switch state	2000
Phase switch states per phase cycle	4
Phase switch cycles per integration	250
Active Switches {none, A, B, both}	Both
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{500,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	~0 (no receiver connected)
ADC Delay	Best value
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

From the FITS files, plot the raw data and check that we get the appropriate waveform (zero level, because the bins contain the same integrated data) plus noise (recall that each integration corresponds to 250 x 4 x 2000 "integrated" ADC samples). We should do this both with and without phase-switching enabled.

SECOND TEST:
Put a sinusoidal wave signal into a SINGLE the CCB input port:

Sinusoidal wave (bipolar differential wave, each output with common mode voltage of 2.5V)
Sinusoid freq. (slow sweep) 10 KHz – 1 MHz (<< 10 MHz)
Sinusoid amplitude 5Vpp
78Ω cable impedance (for matching impedance, differential driver with gain = 2)
Digital frequency synthesizers would be preferable. To transform both AC and DC signals into the correct format for the analog inputs we should use the specially modified detector module. Since cross-talk is frequency dependent, we should use a sweep generator for this test, with a slow sweep. We should also do it with a noise generator. It would make most sense to analyze the data on the fly, rather than create large files for later analysis. This would allow us to perform long scans with a very slow sweep.

For all other CCB input ports, put the following DC level (use the same DC source for all of input ports): 217K (~ mid level) 0 Vd

The input DC noise must be << 0.4% Vfs (-47db). Due to impedance matching, we should have less than 19.5mV / 2 = 9.75m V (0.2% Vfs) or -54.2db at the CCB input port (HINT: differential driver has a gain = 2, with 78Ω impedance, to match cable impedance). DC input signal should be stable for more than 1 sec.

Then simply integrate data from all of the other ports, to see if they deviate from zero when the high DC level signal is turned on.

For this test, set the next normal scan configuration: set the two phase-switches as active (2^2=4 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 2000(0.2m sec). Set the integration time ~200m sec, that is 250 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Set ADC delay to the best one. Collect 525 integrations (105 sec). Start the integrations with the High DC Input generator turned off, and the rest of the input port set to mid level. After the first 5 seconds from starting the integrations, turn on the High DC input, while keep integrating samples. Start changing the frequency of the sin wave every 5 seconds, with 1 KHz steps each time (from 10 KHz to 1 Mhz, that is 100 steps).

Normal scan mode:

ADC Samples per phase switch state	2000
Phase switch states per phase cycle	4
Phase switch cycles per integration	250
Active Switches {none, A, B, both}	Both
Closed (phase) switches (at scan start)	None

Cal {Off, Left, Both, Right} integrations	{5250,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	~0 (no receiver connected)
ADC Delay	Best value
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

From the FITS files, plot the raw data and check that we get the appropriate waveform (zero level, because the bins contain the same integrated data) plus noise (recall that each integration corresponds to 250 x 4 x 2000 "integrated" ADC samples). We should do this both with and without phase-switching enabled.

NONE OF THE ABOVE TESTS REQUIRE THE RECEIVER. ALL OF THE FOLLOWING TESTS REQUIRE THE RECEIVER. For all tests with the receiver set the receiver cal control and beam switching control to CCB (not EXT, MCB, or LOCAL).

IX. Test 8: Zero Level with Receiver Attached

The purpose of this test is to measure (and tune if needed & possible) the overall system zero levels. This tuning would be an offline process (there isn't any adjustable component in the hardware). The zero level is defined as the measured signal when the first stage HEMT amplifiers are all turned off.

Connect the receiver to the backend (16 ports and the control lines). Turn off the HEMT amplifiers. In dump configuration acquire some dump data. Also acquire some regular integration data. Record the zero levels. Tune them to zero if they are excessively large & tunable. Also examine the noise properties of the zero level signal for gross problems.

For the dump test, set the following configuration: set dump_lim_reg to 5000. Set none of the phase-switch as active (2^0=1 phase-switch or measures per cycle). Set none of the cal-diode as active. Set the number of samples per phase-switch state to the maximum of 65535 (6.5m sec). Set the integration time ~13m sec, that is 2 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). Set ADC delay to the best one. Always select the same sampler of the same daughter card. Collect at least 15000 dump samples (3 x 13m sec integrations).

Dump mode:

Samp per state	65535

Phase switch states per phase cycle	1
Phase switch cycles per integration	2
Active Switches {none, A, B, both}	None
Closed (phase) switches (at scan start)	None
Cal {Off, Left, Both, Right} integrations	{3,0,0,0}
Cal {rise, fall} flagging	{0,0}
Dump Port	As desired
Dump Max samples	5000
Dump Max integs	3
Round trip delay	~1u sec – 700n. sec
holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC delay	Best value
Sample type {ADC, FAKE}	ADC

Write the streamed dump data to a file. From the file, plot the corresponding raw output series. The objective would be to determine what the RMS value is for zero RF input.

For the normal scan test, set none of the phase-switch as active (2^0=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 1000 (0.1m sec). Set the integration time ~1m sec, that is 10 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Set ADC to the best one. Collect at least 100 integrations (100m sec).

Normal scan mode:

ADC Samples per phase switch state	1000
Phase switch states per phase cycle	1
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	none
Closed (phase) switches (at scan start)	none
Cal {Off, Left, Both, Right} integrations	{100,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC Delay	Best value
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

From the FITS files, plot the corresponding scaled integrations. The objective would be to determine what the RMS value is for zero RF input (in order to scale the integrations

properly, recall that each integration period corresponds to 10 x 1000 “integrated” samples)

X. Test 9: Input load levels; receiver attached

The purpose of these tests is to set the detected power levels at the CCB, to measure all channel Treceivers and Tcals, and to assess the degree of nonlinearity; all with the full system (CCB+Ka band receiver).

For each test, first check the raw ADC power level with a cold (LN2) load in front of the horns. Check that the RMS value for a cold load corresponds to the expected value. Perform any adjustments (offline calibration process) that are needed to establish the nominal gain for this loading level within a few percent. See the spreadsheet for the appropriate level of a cold load.

In dump mode, set dump_lim_reg to 5000. Set none of the phase-switch as active (2^0=1 phase-switch or measures per cycle). Set none of the cal-diode as active. Set the number of samples per phase-switch state to the maximum of 65535 (6.5m sec). Set the integration time ~13m sec, that is 2 cycles per integration period (~ 100n sec x “N° samples” x “N° phase-switch per cycle” x “integ_len_reg”). Set ADC delay to the best one. Always select the same sampler of the same daughter card. Collect at least 15000 dump samples (3 x 13m sec integrations).

Dump mode:

Samp per state	65535
Phase switch states per phase cycle	1
Phase switch cycles per integration	2
Active Switches {none, A, B, both}	none
Closed (phase) switches (at scan start)	none
Cal {Off, Left, Both, Right} integrations	
Cal {rise, fall} flagging	{0,0}
Dump Port	As desired
Dump Max samples	5000
Dump Max integs	3
Round trip delay	~1u sec – 700n. sec
holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC delay	Best value
Sample type {ADC, FAKE}	ADC

Write the streamed dump data to a file. From the file, plot the corresponding raw output series.

In normal scan mode set none of the phase-switch as active (2^0=1 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 1000 (0.1m sec). Set the integration time ~1m sec, that is 10 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Set ADC to the best one. Collect at least 100 integrations (100m sec).

Normal scan mode:

ADC Samples per phase switch state	1000
Phase switch states per phase cycle	1
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	none
Closed (phase) switches (at scan start)	none
Cal {Off, Left, Both, Right} integrations	{100,0,0,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	~1u sec – 700n. sec
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC Delay	Best value
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

From the FITS files, plot the corresponding output series (in order to scale the integrations properly, recall that each integration period corresponds to 10 x 1000 "integrated" samples)

XI. Test 10: Measure phase switch settle time & round trip delay (w/receiver)

The purpose of this test is to determine the settling times of the phase switches in the receiver, and the round-trip delay of the control signal. We propose two methods to be conducted in parallel: one is to look at the oscilloscope to directly see the response to a phase switch transition; the other is to do a dump. Only the second is useful for determining the round trip delay.

Connect a fast oscilloscope to one of the output receiver channels. Connect the control cable from the CCB to the receiver. Put a stable load in front of the receiver. We assume that intrinsic receiver imbalances and load temperature gradients will generate a large enough difference signal to see the phase switch transition, but if this isn't the case one

cal diode can be turned on. Connect another receiver output channels to the CCB (same daughter card used to connect the scope).

In dump mode set dump_lim_reg to 16000. Set just one of the phase-switch as active (2^1=2 phase-switch or measures per cycle). Set the number of samples per phase-switch state to 2000 (0.2m sec). This gives us enough time to track the settling time for the worst-case scenario (blank_dt_reg register has 8 bits, therefore this means that we have a maximum of 256 x 100n sec blanking period or 256 samples). Set the integration time ~2m sec, that is 5 cycles per integration period (~ 100n sec x "N° samples" x "N° phase-switch per cycle" x "integ_len_reg"). No cal-diode set. Verify that the previous states of both switches are 0 (off). Always select the same sampler of the same daughter card. Set ADC delay to the best one. Collect at least 16000 dump samples (1 x 2m sec integration).

Dump mode:

Samp per state	2000
Phase switch states per phase cycle	2
Phase switch cycles per integration	5
Active Switches {none, A, B, both}	A (then repeat the test with B)
Closed (phase) switches (at scan start)	none
Cal {Off, Left, Both, Right} integrations	{1,0,0,0}
Cal {rise, fall} flagging	{0,0}
Dump Port	As desired
Dump Max samples	16000
Dump Max integs	1
Round trip delay	
holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC delay	Best value
Sample type {ADC, FAKE}	ADC

From the oscilloscope, plot the response of one single phase-switch (or an entire 2m sec integration if the time frame is too short). The objective would be to determine what the settling time is for a single phase-switch (probably the 1/e response point or something like that). This will determine the phase switch blanking time.

Write the streamed dump data to a file. From the file, plot the corresponding raw samples (ADC sequence v/s time). Cross check the settling time seen in the raw ADC data with that seen on the scope. The delay in samples between the start of the first integration and the first phase switch transition visible in the data is the round trip delay.

Do this test with both phase switches, one at a time, to check if there are differences between their correspondent settling times.

Note:

Keep in mind to not change the previous state f the phase-switches (so we don't add an extra roundtrip delay to account the "new" initial start state). In addition, ideally, the start-scan command should be timed to arrive more than one second before the requested time (so there will not extra delay due to SW latency).

Because we know that each phase-switch should last 100 nsec x number of samples per phase-switch, with one active phase-switch the roundtrip delay will be the delay between the (known) start time of the integration, and the first effect of the changing phase-switch to account the initial integration state.

XII. Test 11: Measure cal diode rise & fall times

The purpose of this test is to characterize the cal diode output as a function of time and its repeatability. Since the cals aren't blanked, but merely flagged, and this happens on an integration by integration basis, only fairly low time resolution is needed. Since the cals may have a tendency to change on arbitrary timescales at a low level, the main goal is to identify if there is a significant, rapid "turn-on" response; to assess overall repeatability of the cal signal v/s time; and to measure the "turn-off" time.

Set up the CCB in its nominal integration configuration, but with a) 1ms integration time; b) each of the cals on for much integration (say, a few seconds). Do a scan that lasts several cal cycles. Do several such scans. Compare the time response of each of the cal diodes.

Normal scan mode:

ADC Samples per phase switch state	1000
Phase switch states per phase cycle	1
Phase switch cycles per integration	10
Active Switches {none, A, B, both}	none
Closed (phase) switches (at scan start)	none
Cal {Off, Left, Both, Right} integrations	{100, 5000,0,0}, {100,0,0,500}, {100,0,500,0}
Cal {rise, fall} flagging	{0,0}
Round trip delay	
Holdoff	7 (or 0.2m sec)
Phase switch delay	0
ADC Delay	Best one
Active ports	All (or as desired)
Sample type {ADC, FAKE}	ADC

Therefore, because with one cal-diode commanded to be active and according to the step defined above, we know that after 100m sec, it should be turned on, and then the

roundtrip delay will be the between this time until you see the first effect of the cal-diode active.

XIII. Test 12: Measure 16 Tsys & Tcal values and assess total system linearity, and feed crosstalk

Set up the nominal integration configuration. Data will be acquired from all 16 ports in standard integration mode.

Perform a standard Tsys measurement with hot and cold loads. Use the nominal test configuration and normal integration mode; however, set up the Cal Firing pattern as:

- Cal Off: 10 integrations
- Left Cal On: 5 integrations
- Both Cals On: 5 integrations
- Right Cal On: 5 integrations.

This will result in Tsys for all 16 channels. From the cold load data, and knowing Tsys, determine Tcal values for Right and Left channels, as well as leakage for all 16 channels. Cross check this against the "Both cal" data.

By comparing the magnitude of the cal increment (cal on –cal off) in counts seen against the cold load, v/s that seen against the hot load assess the degree of nonlinearity in the system as a whole.

Quantify the amount of cross-talk between receiver feeds in each of the 16 channels by looking at the cal signal seen when the cal is on in the opposite feed than the port nominally sees.

XIV. Test 13: Noise statistics with receiver

Configure the CCB in its nominal integration configuration, but with: both phase switches active; some cal phases; 0.1 sec integrations; and the best values of round trip and ADC delays. Put a cold load in front of the receiver.

Acquire a 15 minute scan of data (15 x 60 x 10 = 9000 "0.1 sec" integrations). Process the data as follows: For different values of N (N = 90, 900), select N integrations and form the differenced data from the total pool of integrations (therefore you will have M_N groups, with N x M_N = total number of integrations), then calculate the average of each individual group (M_N averages). After that, determine the RMS of the group averages for the same N (one for each different N value). Then, plot the RMS of every group averages v/s N. We should check that the RMS of the group goes down according to $1/\sqrt{(N)}$, with N = number of integrations.

Compute the RMS of the individual differenced samples and compare with the radiometer equation. **These two tests are the crucial tests of whether the CCB + Ka band do what they are designed to do.**

From the radiometer equation, the minimum achievable noise level is given by:

$\sigma = \sqrt{2} \times Tsys / \sqrt{(\Delta B \times \tau)}$

Because the noise power is proportional to the system noise temperature, and the system noise temperature is proportional to the ADC output (samplers), we can write the equation as follow:

$RMS(ADC\ counts) = \sqrt{2} \times Avg\ [ADC\ counts - ADC(zero\ level)\ counts] / \sqrt{(\Delta B \times \tau)}$

Where:
ADC counts = counts for the actual ADC sample (related to the cold input load)
ADC(zero level) counts = counts for the zero level input (see test 6)
ΔB = bandwidth (3.5 GHz)
τ = total integration time spent in each phase-switch state (sec)

Note if you have one phase switch active, τ is equal to the integration time you set in CLEO minus any blanking. If you have two phase switches active τ is twice that since you have averaged two phase-bins to get the SIGNAL phase (feed 1 say), and two phase bins to get the REFERENCE phase (feed 2 say).

Our target is to be within 10% or so of the minimum achievable noise level given by the radiometer equation. If it is a factor of 5 over the theoretical value the CCB probably isn't a significant improvement over the DCR (though I would have to work out the equal-sensitivity point more carefully).

As a sanity check, try 1 sec and 1m sec integration times and see that things behave as expected, in this case also---i.e., the individual integrations differenced RMS relates as sqrt(1/3):1:sqrt(30) for 1000:100:1m sec integrations, roughly.

Also (with 0.1 sec integrations) try 1 kHz (5000 samples per phase-switch), 5 kHz (1000 samples per phase-switch), & 10 kHz (500 samples per phase-switch) switching rates to see if the performance varies with this dimension.

Note:

If we do not have ADC counts, we could use some other integer number, that's scaled & accumulated from ADC counts (we could use the count/voltage gain or the Kelvin/voltage gain).

XV. Test 14: RFI Qualification

The CCB must receive the Interference Protection Group's blessing to be installed on the GBT. There are standard and straightforward procedures for making these measurements in the anechoic chamber. The only potentially tricky part we see is getting the signals we need to operate the CCB, without introducing further RFI. In the anechoic chamber the CCB will need some or all of the following:

- Power (5VDIG, 8VANA, 12VFAN / we should specify the power connector?)
- 1pps
- 10 MHz reference (should we use the same type of cables for the 1 PPS and the 10 MHz clock you have at the GBT receiver room?).
- Fiber Ethernet (ST connector, already in place in the chamber)
- BNC Terminations of the appropriate impedance for the CCB input ports
- DB15 Terminations of the appropriate impedance for the receiver control output port

Set up the nominal integration configuration and acquire a scan of data in normal integration mode. Verify RFI is below limits.

Note:

The CCB needs the 10MHz clock to clock all the FPGAs. So it will be not be able to work without the 10MHz clock. On the other hand, according to Martin the 1 PPS clock is used by the EPP driver and every time you set a scan configuration in sync with the 1PPS clock. Therefore, we will need both signals in the chamber.